uniqarta®

Massively Parallel Laser-Enabled Transfer Technology for Heterogeneous Integration of High-Density SoC/SiP

NEXTFLEX
America's Flexible Hybrid Electronics Manufacturing Institute

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CTO and Founder
UNIQARTA, INC

The Company

- North Dakota SU (Fargo, ND) spin-off
- Registered Nov 2013
  - Locations in Cambridge, MA and Fargo, ND
- Current R&D projects totaling ~$1.8M
- Focus: technology development
  - “Smart Paper”
  - Technologies for ultra-thin, flexible electronics
  - Laser technologies for extremely high-rate assembly of micro- and mini-LEDs
    - Heterogeneous integration of chiplets

DARPA CHIPS

- Concept:
  - Different functionalities segregated into small chiplets (IP blocks), which are then combined onto an interposer
- Supporting Technologies:
  - Design tools
  - IP blocks
  - Assembly methods
    - Fine pitch interconnects
    - Heterogeneous integration: small device handling, multi-device technology processing

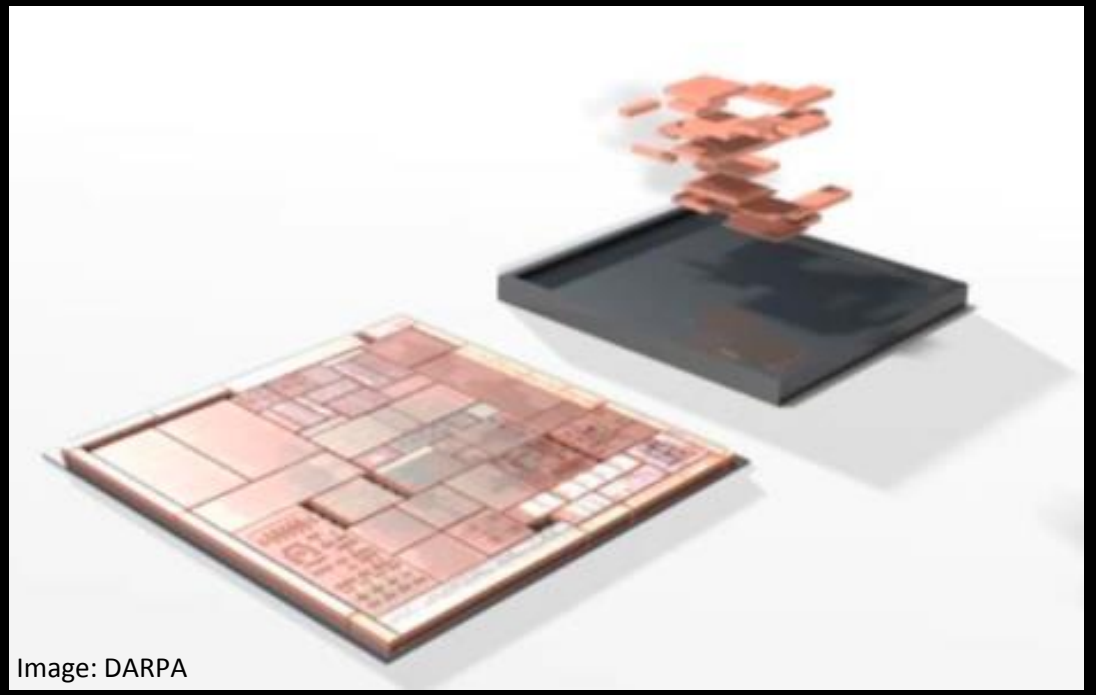
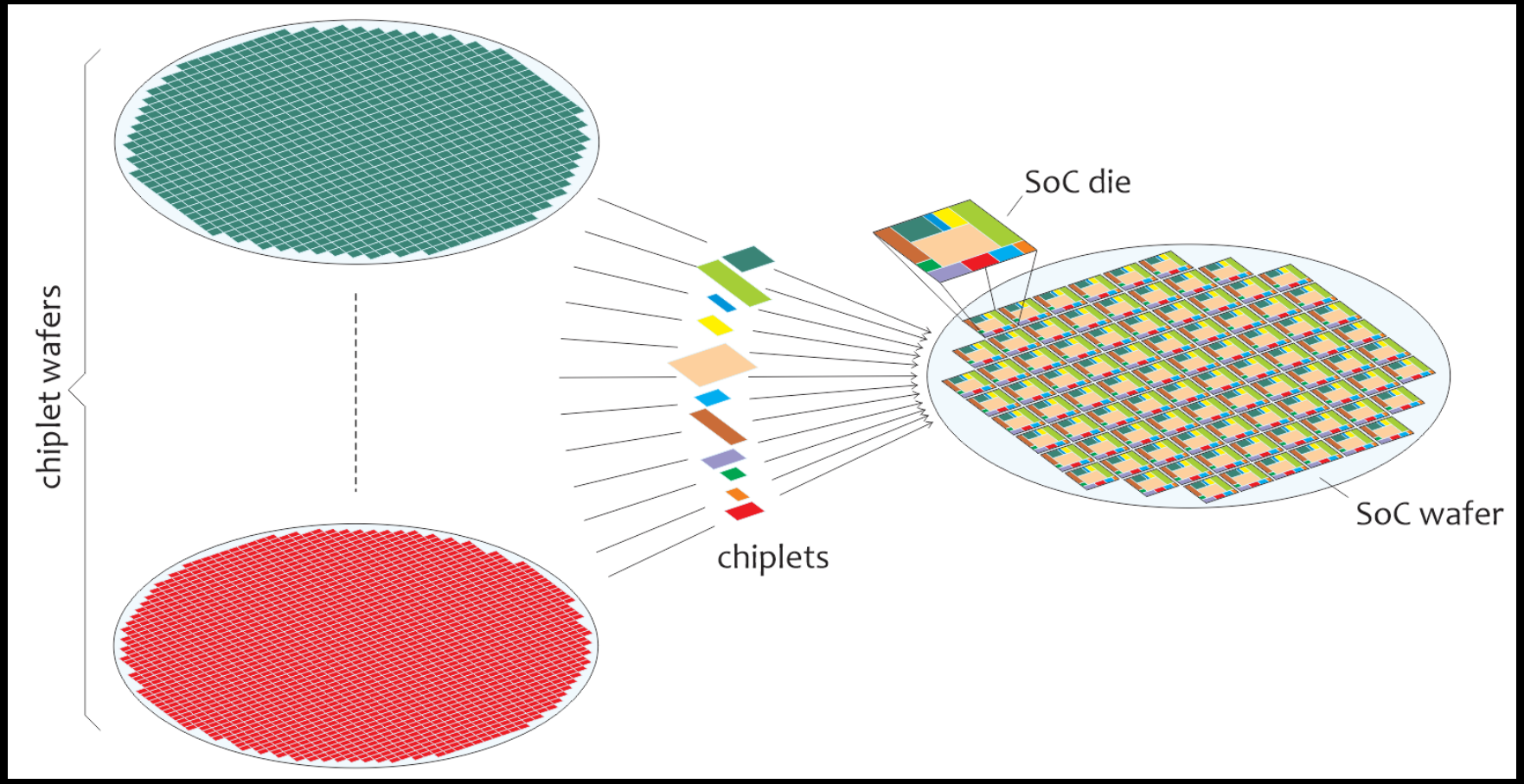


Image: DARPA

Chiplets Wafers → SoC Wafer



Some examples for use in the next slides…

- SoC 1:
  - 6×6 mm^2 ASIC
  - 9 2×2 mm^2 chiplets
  - 1600 ASICs on a 12-in wafer
  - 14,400 chiplets
- SoC 2:
  - 6×6 mm^2 ASIC
  - 144 0.5×0.5 mm^2 chiplets
  - 1600 ASICs on a 12-in wafer
  - 230,400 chiplets

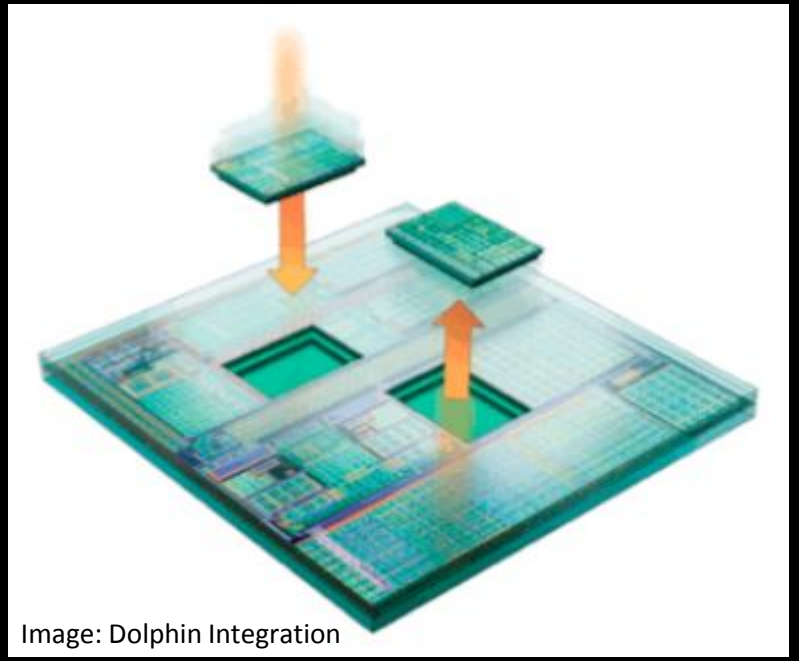


Image: Dolphin Integration

How to put together all these chiplets?

- High-speed flip-chip die bonder: assume a cycle time of 0.5 s (7,200 uph)
  - SOC 1 wafer needs 2 hr to assemble
  - SOC 2 wafer needs 32 hr to assemble!
- A radically different approach is needed for chiplet assembly

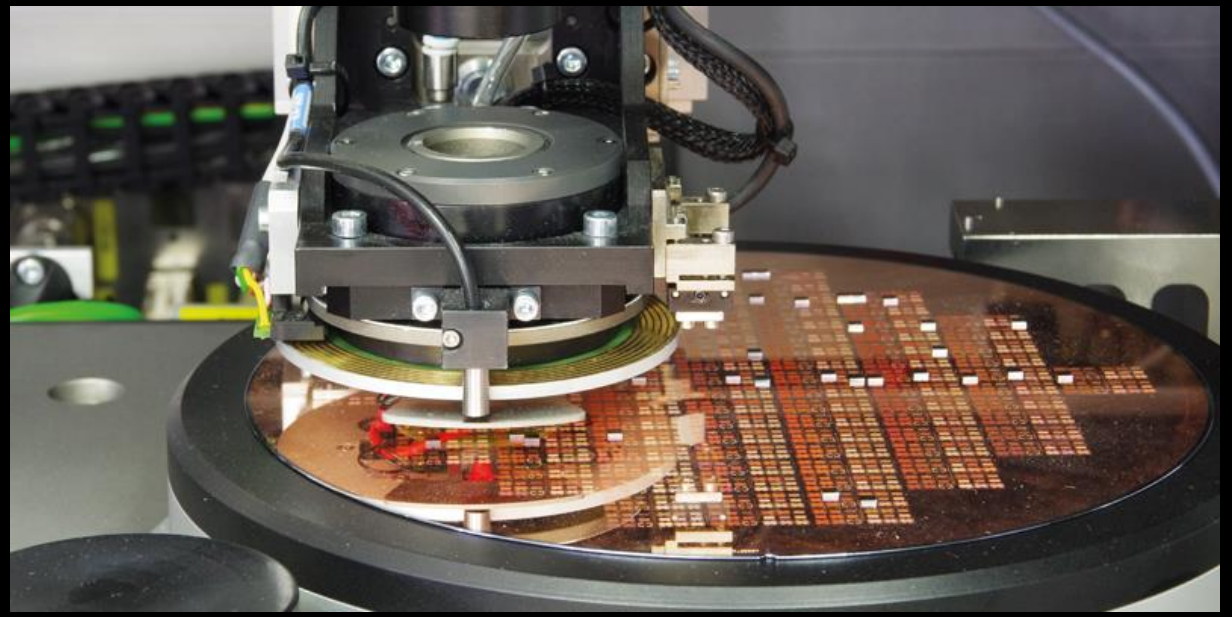
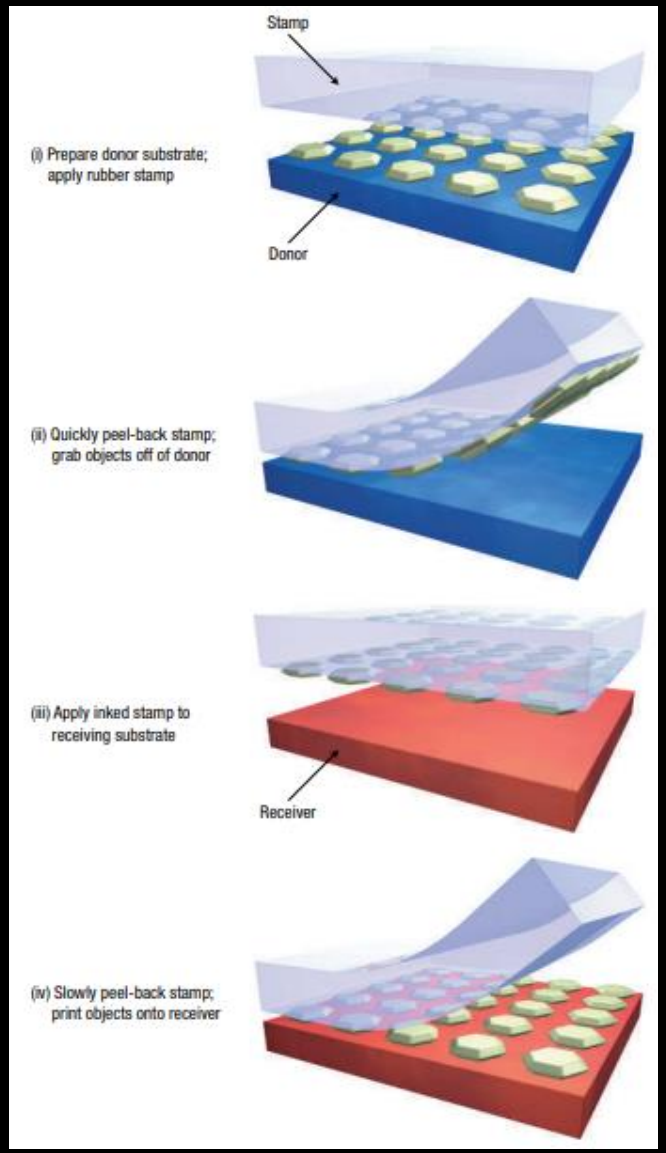


Image: Amicra

Micro-Transfer Printing, µTP

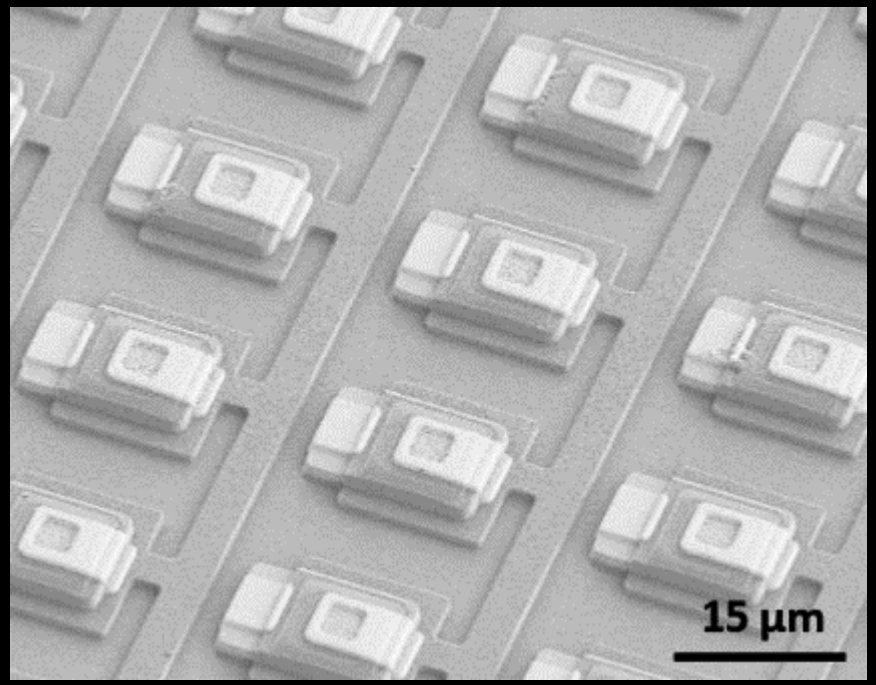
- Relies on kinetically controlled adhesion to pick and place dies: the PDMS stamp moves at high speed during pick-up and low speed during placement
- Capable of transfer rates of M/uph



Meitl, A.M. eta al., Transfer printing by kinetic control of adhesion to an elastomeric stamp. Nature Materials V. 5, pp 33–38 (2006)

However…

- µTP cannot efficiently handle defective chiplets
- CTE mismatch between the PDMS stamp and the Si substrate may be a problem
- Requires specially prepared wafers: chiplets attached using tethers to allow for pick up by the stamp's relatively weak adhesion
- Question: will fabs be willing to change their entire CMOS process flow to accommodate the µTP requirements?
- There is a need, therefore, for assembly technologies that are compatible with traditional silicon chip processing.

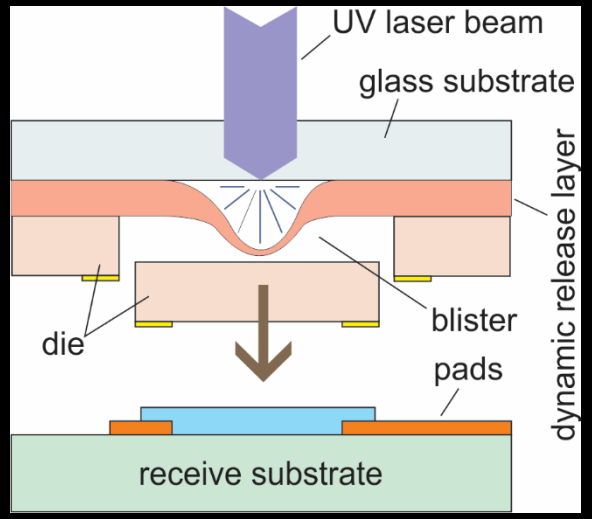


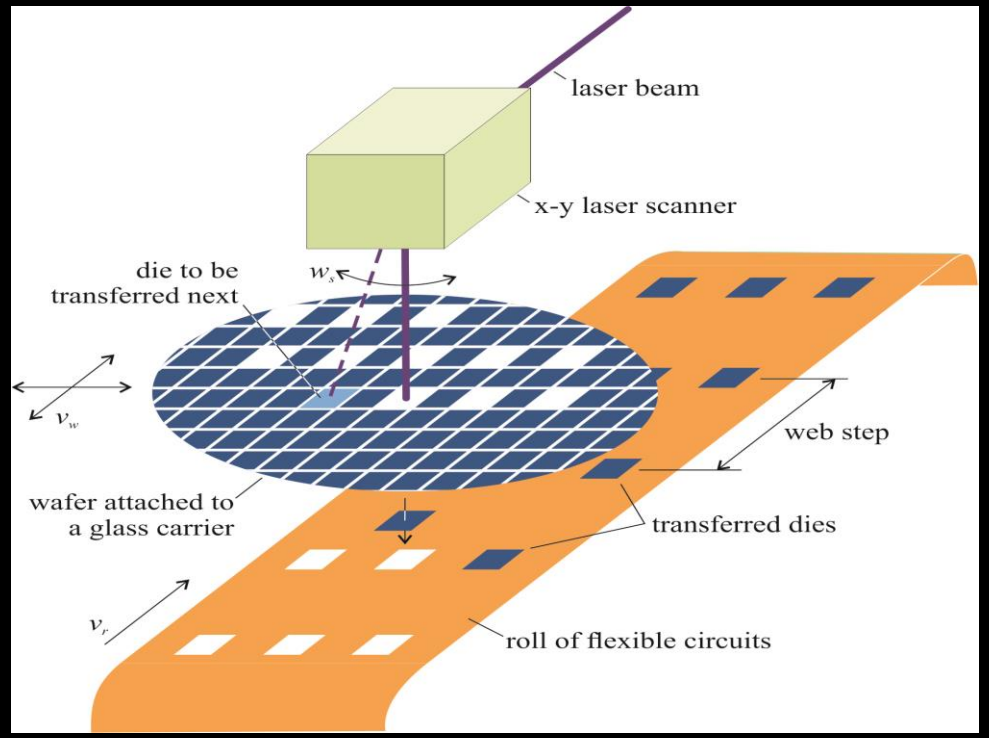
Radauscher, E.J., et al. Miniaturized LEDs for Flat-Panel Displays. SPIE Proc. 10124, 2017

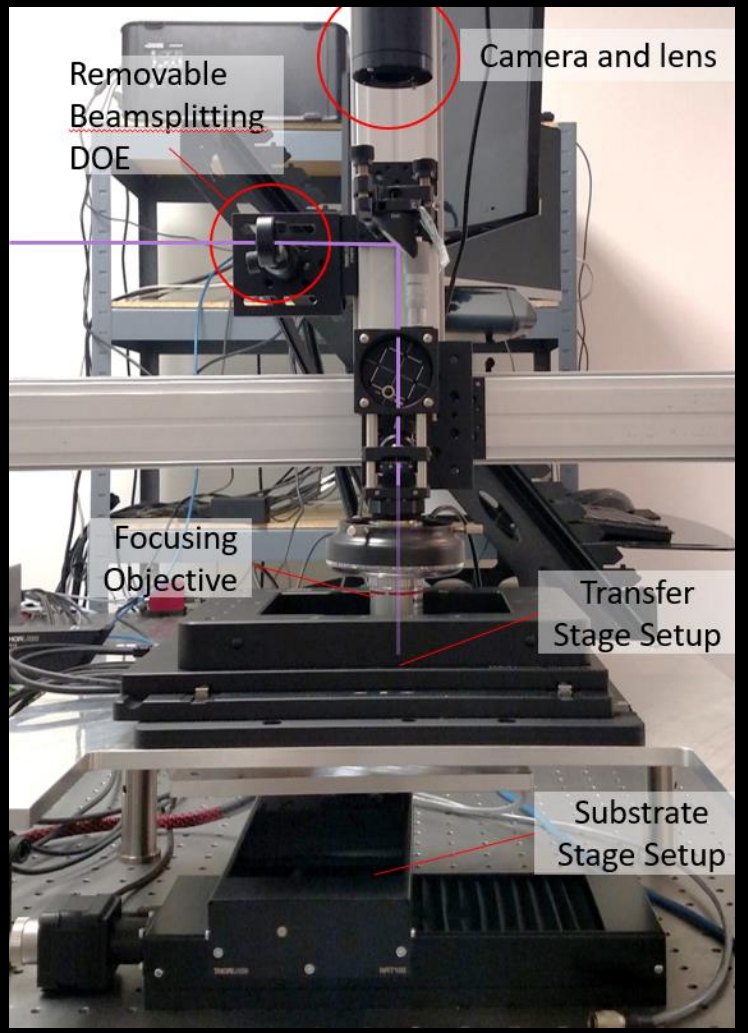
Uniqarta's LEAP Technology

LEAP = Laser-Enabled Advanced Placement

- Ultra-fast placement (>100M uph)
- Known Good Die selectivity
- Wide range of component types (Si, GaN, AlN, sapphire, metal…) and sizes (20 µm to tens of mm)



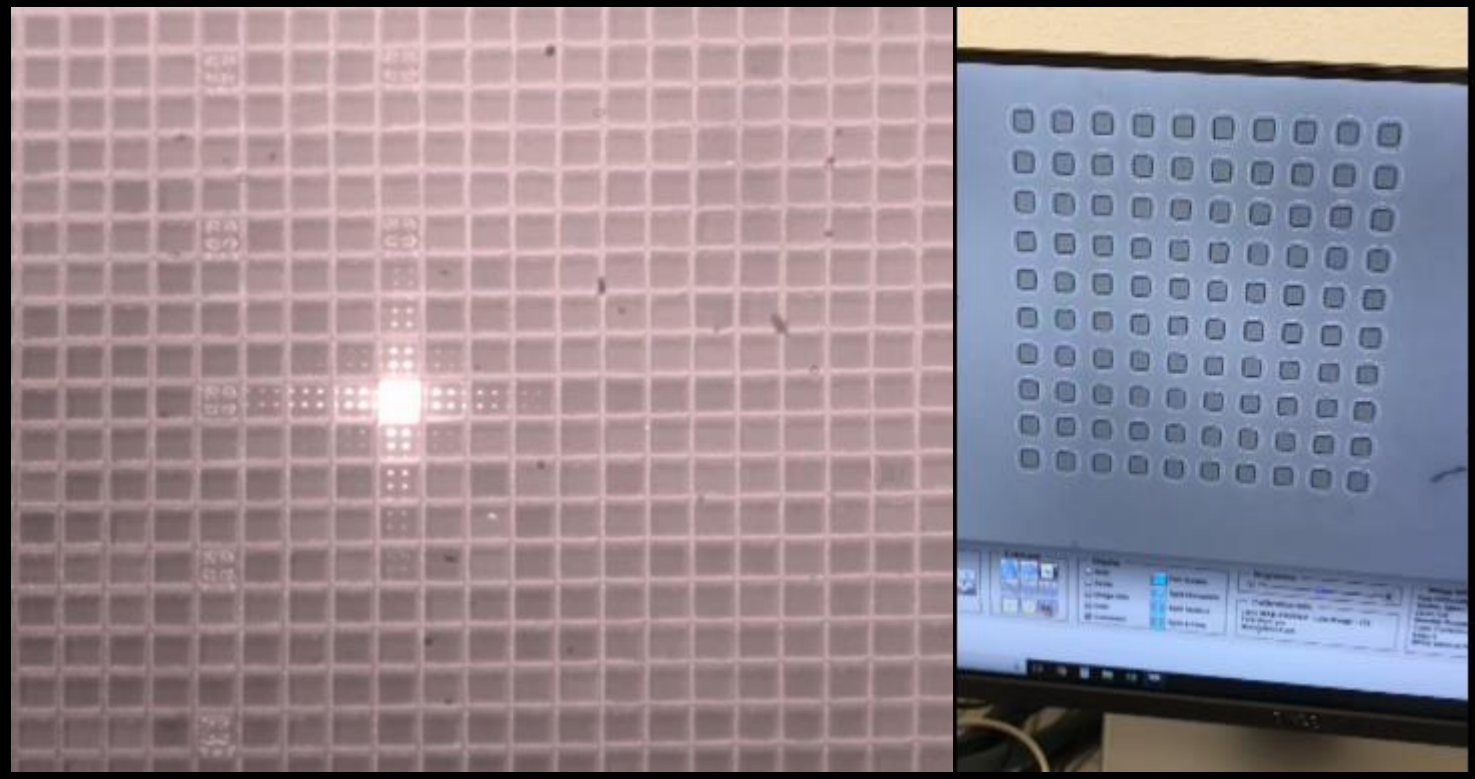




US 9,862,141; JP 6053756; CN ZL2012800270480; EP 2697822; KR 1020140045936,…

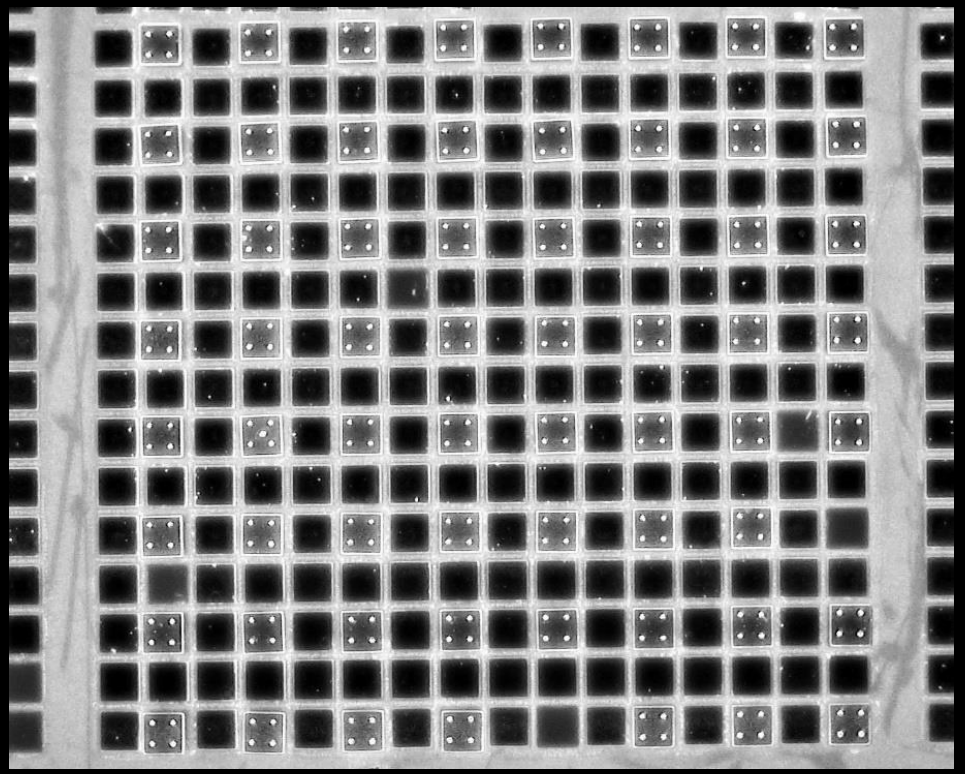
LEAP in a Single-Die Transfer (SDT) Mode

Demo: 1,040 ups (3.7M uph)



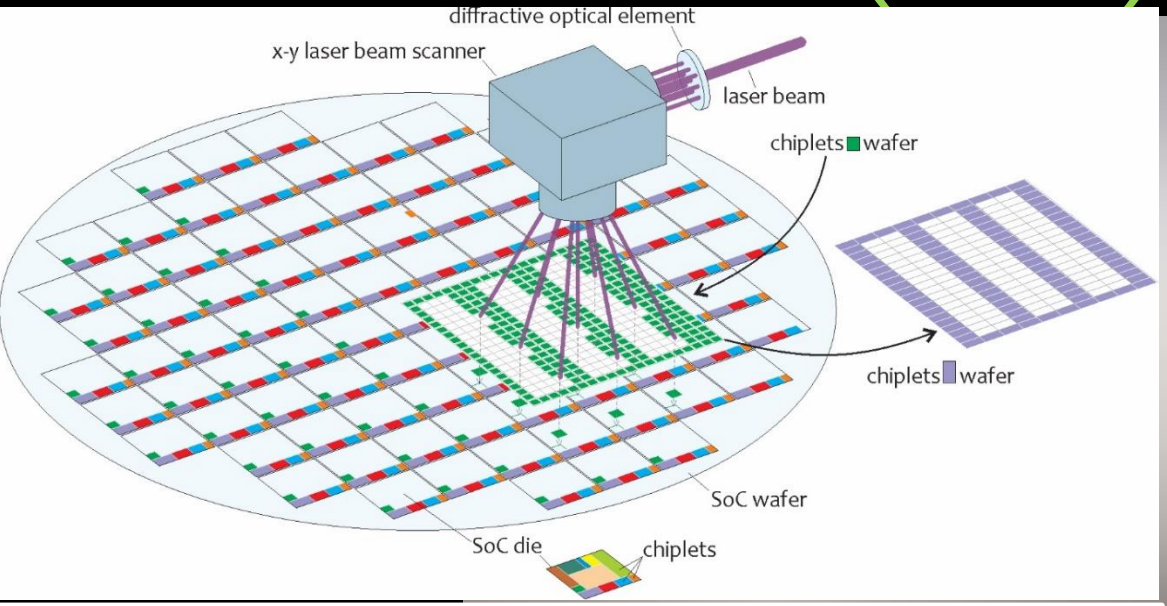
- 100 laser pulses, 100 transferred dies
- 1 die transferred per pulse
- 96 ms

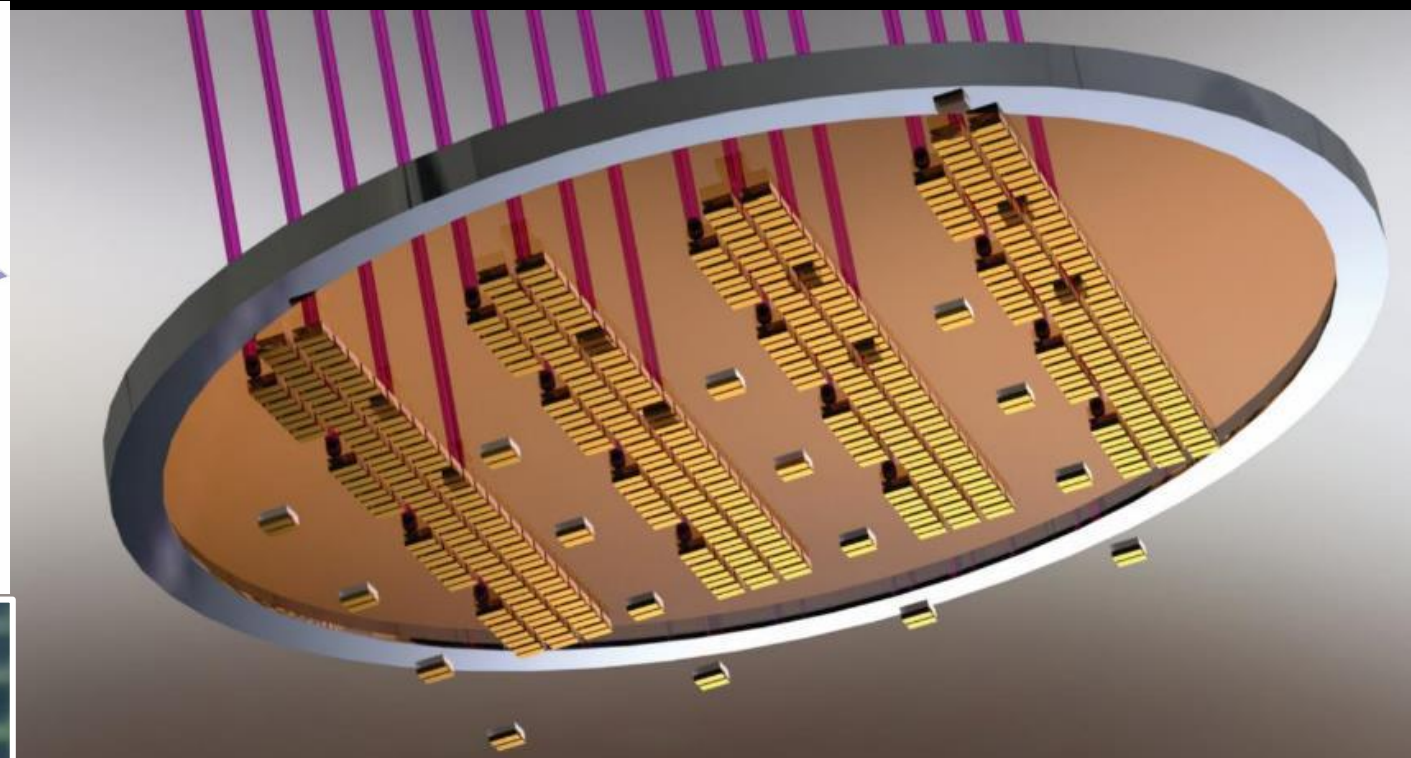
LEAP is not only very fast but also precise

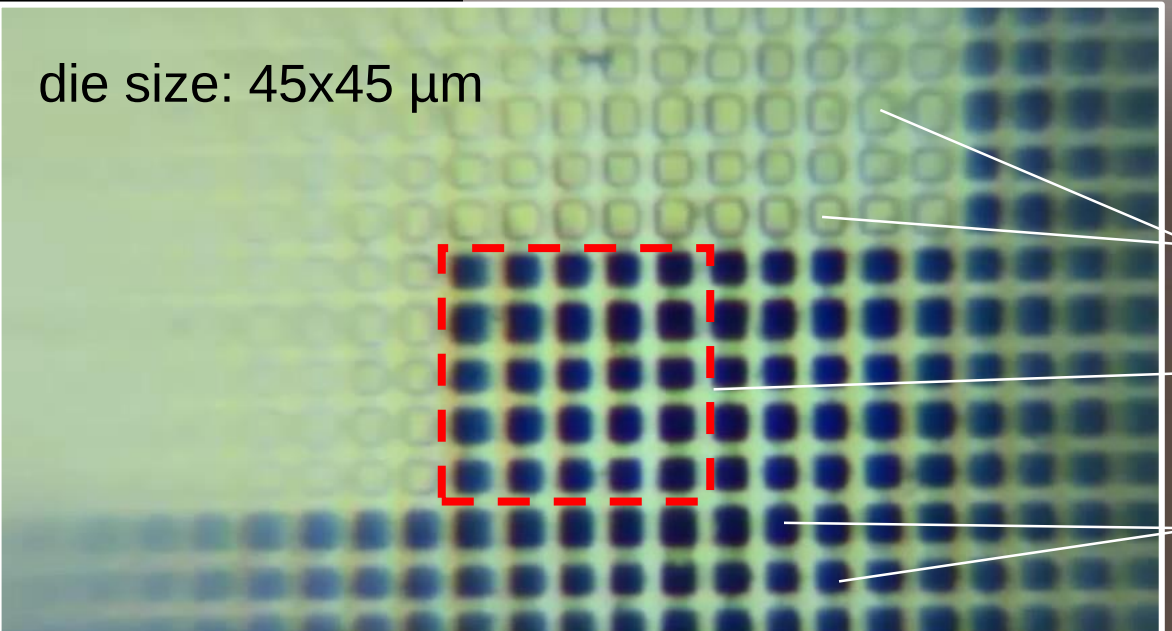


A field of transferred 50×50 µm dies
(image taken through the glass carrier)

Uniqarta's Ultra-Fast Placement Solution:
Milti-Die Transfer (MDT)







locations of previously transferred dies

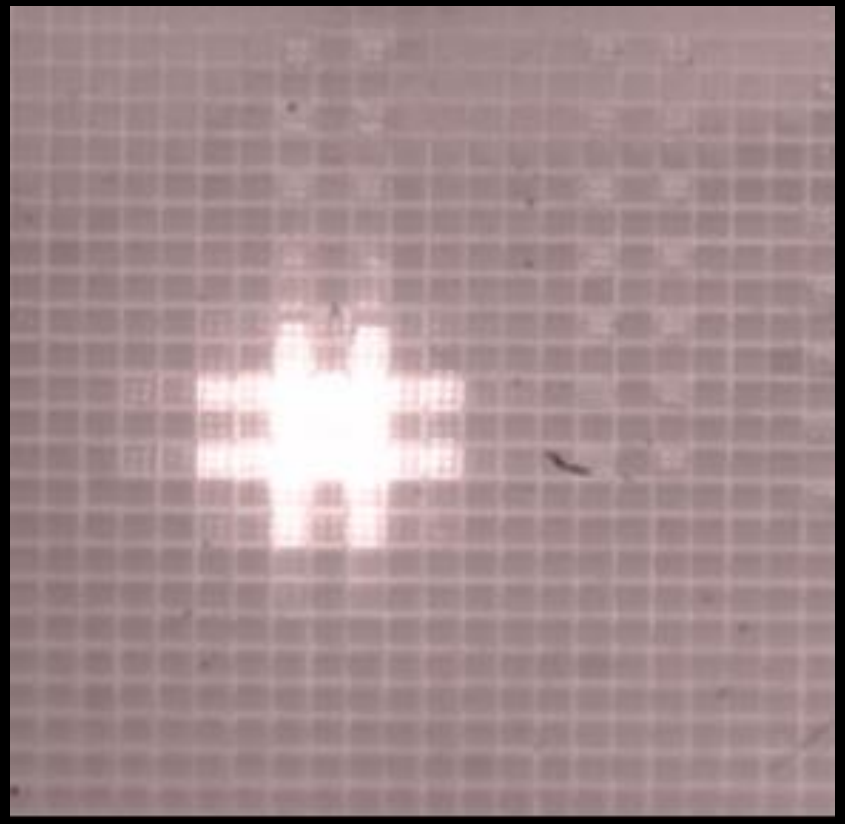
5x5 array to be transferred

untransferred dies on carrier underside

WO2017123780; US 62/518270; TW 201725642

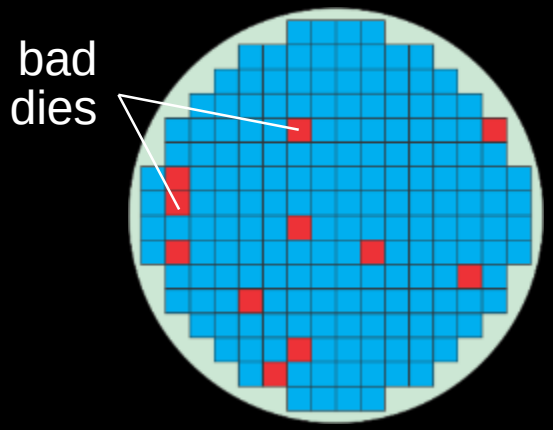
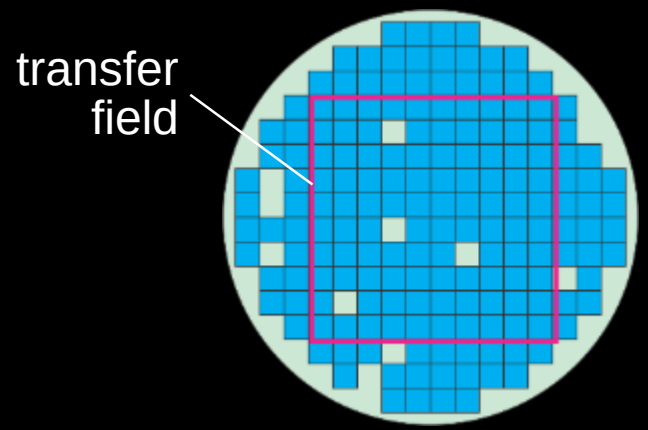
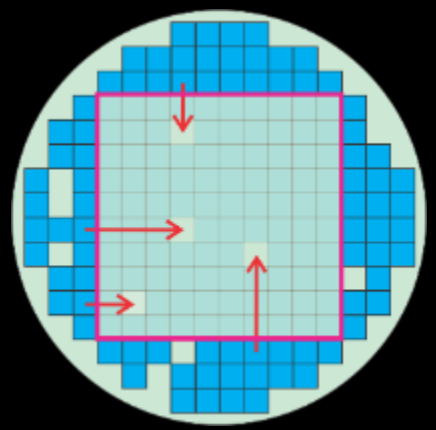
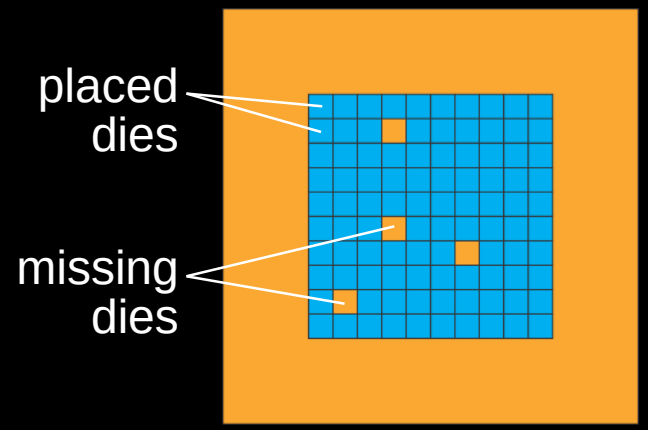
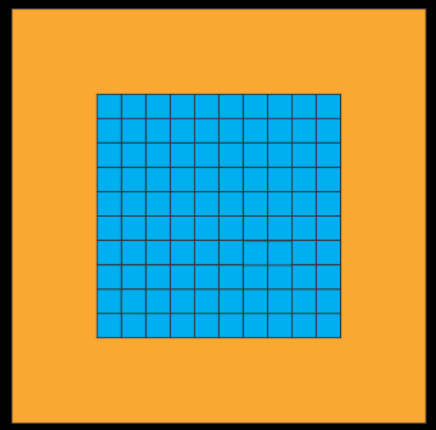
LEAP in a Multi-Die Transfer Mode

Demo: 2x2 MDT; 3,500 /s (12.6M uph)



- 16 laser pulses, 64 transferred dies
- 4 dies transferred per pulse
- 18 ms

SDT and MDT used for Good-Die-Only Placement

	1. Bad Die Removal *single-die mode*	2. Good Die Placement *multi-die mode*	3. Fill-In *single-die mode*
Wafer			
Substrate	(none)		

Thank you.